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Performance Analysis of Germanium P-Channel Junctionless FinFET for Low Power and High Performance Applications

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Abstract

In this paper, the performance of germanium (Ge) p-channel Junctionless (JL) FinFET has been compared with silicon (Si) p-channel JL-FinFET. The device performance was evaluated in terms of sub-threshold swing, threshold voltage, on current, gate capacitor, intrinsic delay, power dissipation and power delay product for present technology. The use of Ge in JL-FinFET improves 64% delay over Si counterpart when both devices have the same off current at 100pA/um.

Keywords: Junctionless (JL) FinFET, germanium (Ge), silicon (Si), sub-threshold swing (SS), threshold voltage (V_{TH}), on current (I_{ON}), off current (I_{OFF}), delay, power dissipation, power-delay-product (PDP).

1. Introduction

As per Moore's law [1], aggressive down scaling of device dimension of conventional metal-oxide-semiconductor field effect transistor (MOSFET) offers various problems, including the production of ultra-sharp source/drain junctions. Downscaling increases short channel effects in device which further enhances leakage current as well as power dissipation. A junctionless transistor (JLT) [2] has been developed as a solution to this problem, and it shows significant potential for future technology nodes. JLT has the same doping type and concentration in the source, channel, and drain regions, which denotes the absence of junction in such devices. In compared to its conventional counterpart, a JLT has higher short-channel immunity [3], improved drain-induced barrier lowering (DIBL) [3], lower electric field in the on-state [4], steep sub-threshold slope [5], and improved both analog [6] and digital logic [7] performances.

For further improvement, FinFET technology has come to improve the short channel immunity by increasing the gate control of conventional MOSFET. Recently, different research groups are working on different types of advanced devices to get higher performance and lower power dissipation in CMOS technology. To enhance the speed of the device, higher mobility Ge material may be used as a p-type channel material [8]. It is reported that Ge channel devices has been simply integrated into Si process technology. High drive current [9], outstanding I_{ON} to I_{OFF} ratio [10] and impressive immunity to control short-channel effects (SCEs) [11] have been already reported in Ge-on-insulator (GeOI) devices.

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JL-FinFET on GeOI has been studied recently [12-15] in order to integrate the intrinsic qualities of Ge with the good features of JLT. Additionally Ge JL-FinFET provides better immunity against random-discrete-dopant induced threshold voltage fluctuation [16].

In this paper, we have investigated some device characteristics of Ge p-channel JL-FinFET in comparison with Si p-channel JL-FinFET. To understand and analyze the device performance of aforementioned devices, node 10nm technology of IRDS 2017 [17] has been considered.

2. Device structure and simulation

Sentaurus TCAD [18] has been used to simulate all the device characteristics for this study. Figure 1 shows the schematic view of JL-FinFET. As per International roadmap for device and systems (IRDS) we have chosen node 10nm technology [17] to evaluate all the device performances. The channel length is valued as 22nm, channel width as 8nm, channel height as 45nm, effective oxide thickness (EOT) as 0.9nm, doping concentration of source, channel and drain is 4×10^{19} atoms/cm^3. The work function (WF) of gate metal for different devices has been optimized to obtain a leakage current I_{OFF} at 100 pA/μm in accordance with IRDS 2017. Here, 0.75V has been used as bias voltage to study the device characteristics.

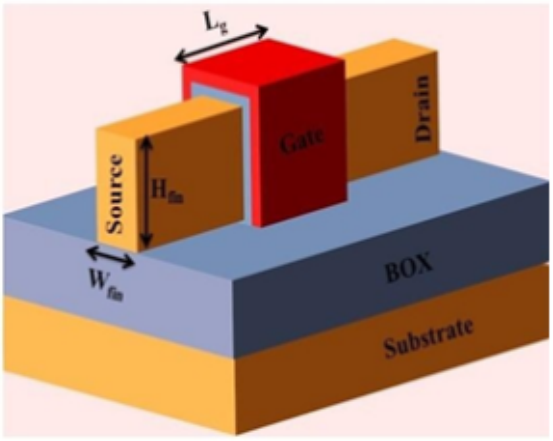

Figure 1: Schematic view of JL-FinFET using TCAD simulator

Sentaurus 3D numerical device simulator [18], version H-201703.03, is used to simulate all of the device characteristics. In our simulations, doping dependent, quantum density gradient, high field saturation, normal field-dependent mobility models, quantum density gradient, Hurkx's band-to-band, Shockley–Read–Hall (SRH) recombination, and band gap narrowing (BGN) models have been used. Coulomb and neutral defect scattering effects are added with μ_L (low-field bulk mobility) [19] for model calibration, and default values of μ_L [20-21] are modified. The modified values of μ_L are 80.5 and 300 $m^2V^{-1}s^{-1}$ [22] for Si p-channel JL-FinFET and Ge p-channel JL-FinFET, respectively. All the calibrated models for Si p-channel and Ge p-channel JL-FinFETs are reported in ref. [7] against the experimental results [23].

3. Result and discussions

According to IRDS 2017, Figure 2 depicts the transfer characteristics (I_D-V_G graph) of Si p-channel and

Ge p-channel JL-FinFETs for node 10nm technology. Figure 3 shows the variation of gate capacitances as a function of gate voltage using ac analysis. Figure 4 shows different device parameters for both type of devices. When V_{GS}=V_{DS}=0.75V, drive current (I_{ON}) is calculated from Figure 2. Ge p-channel will give an 84% improvement in drive current over the Si p-channel as Ge offers higher carrier mobility than Si. Next, the Sub-threshold Swing (SS) is also calculated using the transfer characteristics and shown in Figure 4.

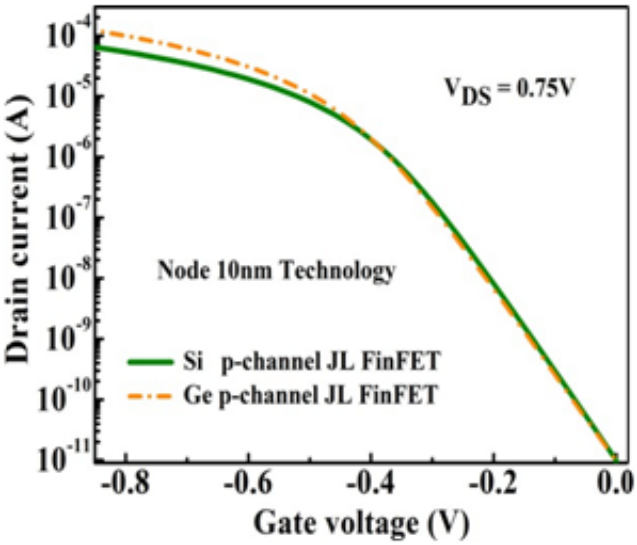

Figure 2: $I_D$vsV_G characteristics for both type of devices

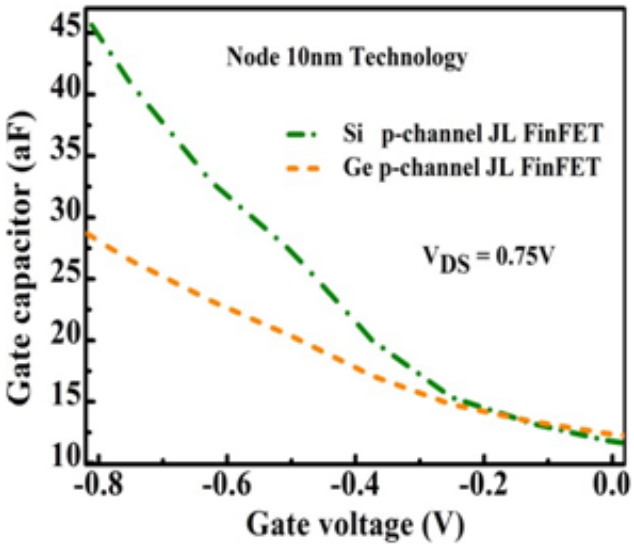

Figure 3: C_{gg}vsV_G characteristics for both type of devices

Both devices provide nearly comparable SS, as illustrated in Figure 4. Different device parameters like threshold voltage (V_{TH}), delay, static power dissipation (P_{Static}), dynamic power dissipation ($P_{Dynamic}$) and power delay product (PDP) are listed in Table 1. In comparison to Si p-channel JL-FinFET, Ge p-channel JL-FinFET has a slightly higher V_{TH}. As per Figure 4, it is clear that Ge provides more or less double on current and lower gate capacitance compared with Si when both devices have identical SS. As a result, Ge p-channel JL-FinFET with lower gate capacitance and higher on current provides 64% improvement in terms of intrinsic delay as intrinsic delay is measured by the CV/I metric. Thus Ge opens a path to minimize the delay of the device.

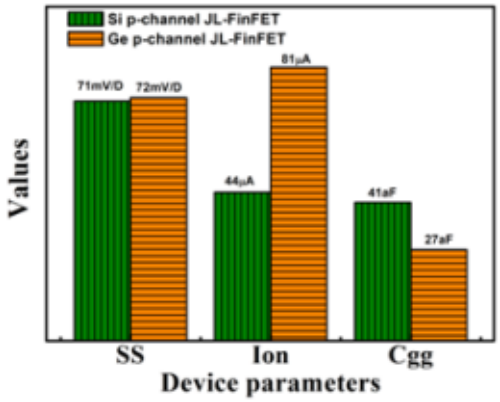

Figure 4: Different device parameters for both type of devices

Table 1: Performance parameters for both type of devices

Parameters	P-channel Si JL-FinFet	P-channel Ge JL-FinFET
V_{TH}(mV)	**333**	**338**
Delay(ps)	**0.7**	**0.25**
P_{Static}(pW)	**7.35**	**7.35**
$P_{Dynamic}$(μW)	**33**	**61**
PDP(aJ)	**23**	**15.3**

The static power dissipation ($P_{Static} = I_{OFF} . V_{DD}$) is identical because both devices have the same off current at 100pA/μm, however the dynamic power dissipation is different. The value of dynamic power dissipation ($P_{Dynamic} = C_L V_{DD}^2 f$) is affected by both the load capacitor and frequency. The values of dynamic power dissipation are estimated and reflected in Table 1, assuming $C_L = C_{gg}$ and f=1/delay. In comparison to Si, the Ge provides lower delay and higher but it increases dynamic power dissipation. Though Ge offers higher dynamic power dissipation, the interesting part is, due to lower intrinsic delay of Ge JL-FinFET, it decreases the overall power delay product (PDP) compared with Si, as illustrated in Table-I.

4. Conclusion

In comparison to Si counterparts, Ge p-channel JL-FinFETs offer higher on current, lower gate capacitance and lower delay. Sub-threshold swing, threshold voltage and static power dissipation are all the same for both types of devices. Lower delay increases dynamic power dissipation, which is a disadvantage for Ge channel devices, but overall power delay product has been reduced when utilizing Ge. Based on these findings, Ge p-channel JL-FinFETs may be an attractive higher mobility channel material for high performance and low power applications in future.

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